REMARKS

The Office Action dated May 3, 2005 has been received and carefully considered. Reconsideration of the outstanding rejections in the present application therefore is respectfully requested based on the following remarks.

Obviousness Rejections of Claims 1-6 and 8-10

At page 2 of the Office Action, claims 1-5 and 8-10 were rejected under 35 U.S.C. Section 103(a) as being unpatentable over Chang (U.S. Pat. App. Pub. No. 2003/0005247) in view of Hahm (U.S. Patent No. 6,223,646).[1] At page 5 of the Office Action, claim 6 was rejected under 35 U.S.C. Section 103(a) as being unpatentable over Chang in view of Hahm and further in view of Microsoft Computer Dictionary. These rejections are respectfully traversed.

Claim 1, from which claims 2-6 and 8-10 depend, recites the features of when in a first mode of operation, utilizing a first output coupled to a memory to provide a first data lane enable for facilitating access of a portion of a first memory storage location of the memory associated with a first memory address and when in a second mode of operation, utilizing the first output to provide an address bit of a second memory address for facilitating designation of a second memory storage location of the memory. With respect to these features, the Office Action asserts that Chang teaches a memory access system in which the SMI signal "provides a first data lane enable to the SMM 180," where "the SMM utilizes the SMI signal for facilitating access of a portion of a first memory storage location associated with a first memory address within memory 140" and further where the SMI signal is utilized "for facilitating designation of a second memory storage location (addressing range beyond 1 Mbyte) within memory 140." *Office Action*, p. 2. The Office Action then concludes that "[s]ince the two memory modes of Chang denote different address thresholds to be accessed, the first and second modes facilitate access to different memory storage locations and thus provide different address portions." *See Office Action*, pp. 2-3. The Office Action further asserts that the "SMI signal facilitates access in [the Chang system] by providing an interrupt when needed, since this signal comes from one

source, the software interrupt interface 160, the system is utilizing the output of one port to perform at [sic] either mode of operation." *See Id.*

The Office Action acknowledges that "Chang does not teach the output being coupled directly to the memory." *Id.* The Office Action instead improperly relies on Hahm as allegedly disclosing "a memory interface wherein a controlling module (FPGA 100) outputs an enable signal, an address signal, a data signal, a read signal, and write signals and these outputs are directly coupled to a memory 300 (See Figure 1)." *Id.* The Office Action therefore concludes that "it would have been obvious to one of ordinary skill in the art . . . to modify the system of Chang so that its control structure (comprising real mode 100, software interrupt 160, and SMM 180) *are all integrated into a single component performing all appropriate functions*, as in the system of Hahm, *since doing so allows for simplified connectivity. In integrating the components in the system of Chang, the outputs of such a system would be directly coupled to the memory 140*." *Id.*, p. 3 (emphasis added). Contrary to the assertions of the Office Action, the Applicants respectfully submit that the proposed combinations of Chang, Hahm and the Microsoft Computer Dictionary fail to disclose or suggest each and every feature recited by claims 1-6 and 8-10, and further submit that there is no motivation to modify the teachings of Chang in view of Hahm as suggested by the Office Action.

1) Chang and Hahm Fail to Disclose or Suggest an Output that Provides a Data Lane Enable in a First Mode and an Address Bit in a Second Mode

As noted above, the Office Action asserts that the SMI signal of Chang is equivalent or analogous to the first output of claim 1. *See Office Action*, p. 2. As provided by claim 1, the first output is utilized to provide a first data lane enable in a first mode and to provide an address bit in a second mode. In contrast, the SMI signal of Chang is an enable signal or a system management interrupt (SMI) signal that is provided by the chipset 220 (Chang, FIG. 2) to the CPU 200 (Chang, FIG. 2) in order to direct the CPU 200 to enter the system management mode (SMM) and to actuate a SMI handler routine. *See Chang*, para. 0031. Thus, Chang teaches the use of the SMI signal to trigger the initiation of the SMM and SMI hander routine at the CPU

[1] The Final Office Action listed the rejection of claims 1-5, 8-10, 16, 18, 19 as "rejected under 35 U.S.C. 102(e) as being anticipated by Chang . . . in view of Hahm . . . ." The Applicants note that an anticipation rejection typically is improper in view of multiple references. The Applicants therefore provide the following remarks under the assumption that this rejection was intended as an obviousness rejection under 103(a).

200. Chang, however, does not disclose or even suggest that the SMI signal is used to provide an address bit as recited. Hahm provides no disclosure or suggestion that software interrupt signals provided to a CPU, such as the SMI signal of Chang relied on by the Office Action, are used to provide an address bit of a memory address designating a memory storage location of a memory. Accordingly, the proposed combination of Chang and Hahm fails to disclose or suggest the features of utilizing a first output to *provide a first data lane enable* for facilitating access of a portion of a first memory location when in a first mode and utilizing the first output to *provide an address bit* of a second memory address when in a second mode as recited by claim 1.

2) The Proposed Modification of Chang in view of Hahm Does Not Result in a First Output Coupled to a Memory

As provided by claim 1, the first output is utilized to provide a first data lane enable in a first mode and to provide an address bit in a second mode is coupled to a memory. Chang discloses that the SMI signal (which the Office Action asserts is analogous to the first output of claim 1) is connected between the chipset 220 and the CPU 200 (Chang, FIG. 3). Chang provides no disclosure or suggestion that the SMI output of the chipset 220 can be connected to the memory 240. In view of this deficiency in the disclosure of Chang, the Office Action asserts that the system of Chang can be modified in view of the teachings of Hahm to arrive at a system whereby the SMI output of the chipset 220 is coupled to the memory 240. *See Office Action*, p. 3. As discussed above, the SMI signal of Chang is a software interrupt or enable signal that is used to direct the CPU 200 of Chang to enter the SMM mode and to initiate a SMI interrupt handler routine. Hahm merely provides a memory interface that can be integrated into a field programmable gate array (FPGA) and provides no disclosure or suggestion that a software interrupt signal that is provided to a CPU, such as the SMI signal of Chang, also may be provided to a memory. In fact, Hahm does not address interrupt signals in any manner. Moreover, not only is the provision of a software interrupt signal not disclosed or suggested by Hahm, one of ordinary skill in the art would appreciate that there is no reason to provide a software interrupt signal to a memory as a conventional memory (which the memories of Chang and Hahm appear to be) does not implement any sort of software processing capability and therefore would have no use for the software interrupt signal.

The Office Action asserts that Hahm renders obvious to one of ordinary skill in the art the integration of "control structure (comprising real mode 100, software interrupt 160, and SMM 180)" into "a single component performing all appropriate functions," such that by "integrating the components in the system of Chang, the outputs of such a system would be directly coupled to the memory 140." *Office Action*, p. 3. The Applicants respectfully submit that the mere integration of the components of the system of Chang into a single device would not affect the interconnection of the components and therefore would not result in the SMIOUT# pin (which provides the SMI signal) being coupled to the memory 140. Instead, if combined into a single device as proposed, the connections between the components of Chang would remain the same absent some motivation provided by Hahm to alter these connections. Hahm fails to provide such motivation. Accordingly, it is respectfully submitted that the proposed combination of Chang and Hahm fails to disclose or suggest the features of a first output coupled to a memory as recited by claim 1.

3) There is No Motivation to Combine Chang and Hahm

Not only does the proposed combination of Chang and Hahm fail to disclose or suggest features of claim 1, there is no motivation to combine the teachings of Chang and Hahm. The Office Action asserts that the modification of the system of Chang to be implemented as a single device as disclosed by Hahm is motivated by the alleged simplified connectivity resulting from such a device. The Applicants, however, find no mention or suggestion of a desire for simplified connectivity in Chang nor do the Applicants find any mention in Hahm that the implementation of the system of Hahm in a single device results in simplified connectivity. In fact, Hahm does not disclose any particular advantage to implementing the disclosed system in the field programmable gate array (FPGA) 100. Thus, as Chang does not profess a desire for simplified connectivity and as Hahm does not profess that the integration of the components in to the FPGA 100 simplifies connectivity in any manner, it is respectfully submitted that neither Chang nor Hahm provide any support for the Office Action's proposed motivation (i.e., simplified connectivity) to combine their teachings.

Moreover, as discussed above, Chang teaches a system having a CPU 200 connected to a memory 240, where the CPU 200 receives a SMI signal from a chipset 220 and Hahm discloses the incorporation of a number of components into a FPGA. One of ordinary skill in the art will

appreciate that a conventional FPGA cannot implement a CPU and Hahm therefore teaches away from the incorporation of the system of Chang into a single device.

4) The Proposed Combinations of Chang, Hahm and the Microsoft Computer Dictionary Fail to Disclose or Suggest Each and Every Feature of Claims 1-6 and 8-10

As discussed above, there is no motivation to combine the teachings of Chang and Hahm. Even if combined, the proposed combination of Chang and Hahm fails to disclose or suggest at least the features of utilizing a first output to provide a first data lane enable when in a first mode utilizing the first output to provide an address bit of a memory address when in a second mode as provided by claim 1. Moreover, the proposed combination of Chang and Hahm fails to disclose or suggest the features of the first output being coupled to a memory. The Office Action does not assert that the Microsoft Computer Dictionary discloses or suggests these features. Accordingly, it is respectfully submitted that the Office Action fails to establish that the proposed combinations of Chang, Hahm and the Microsoft Computer Dictionary disclose or suggest each and every feature of claim 1, as well as each and every feature of claims 2-6 and 8-10 at least by virtue of their dependency from claim 1. Moreover, these claims recite additional features neither disclosed nor suggested by Chang, Hahm or the Microsoft Computer Dictionary. Consequently, it is respectfully submitted that the obviousness rejections of claims 1-6 and 8-10 are improper at this time and the withdrawal of these rejections therefore is respectfully requested.

Obviousness Rejections of Claims 16-18

At page 2 of the Office Action, claims 16 and 18 were rejected under 35 U.S.C. Section 103(a) as being unpatentable over Chang in view of Hahm. At page 9 of the Office Action, claim 9 was rejected under 35 U.S.C. Section 103(a) as being unpatentable over Chang in view of Hahm and further in view of the IEEE Dictionary. These rejections are respectfully traversed.

Claim 16, from which claims 17 and 18 depend, recites the features of an address control portion having an output to indicate a value of an address bit when in a first mode of operation, a first data lane enable control portion having an output to indicate a first data lane enable value when in the second mode of operation and an output pin coupled to the output of the address control portion and the output of the first data lane enable control portion, and further coupled to

a memory. The Office Action asserts that the proposed combination of Chang and Hahm discloses these features based on a similar line or reasoning discussed above with respect to the rejection of claims 1-5 and 8-10. Specifically, the Office Action asserts that "[t]he SMI signal facilitates access in [the Chang system] *by providing an interrupt when needed*, since this signal comes from one source, the software interrupt interface 160, the system is utilizing the output of one port to perform either mode of operation." *Office Action*, p. 4 (emphasis added). As similarly discussed above, the Office Action acknowledges that Chang does not teach an output pin coupled to memory and therefore relies on the teachings of Hahm. *See Id.* The Office Action concludes that the modification of the system of Chang by the teachings of Hahm is motivated for reasons of "simplified connectivity." *Id.* Contrary to the assertions of the Office Action, the Applicants respectfully submit that the proposed combinations of Chang, Hahm and the IEEE Dictionary fail to disclose or suggest each and every feature recited by claims 16-18, and further submit that there is no motivation to modify the teachings of Chang in view of Hahm as suggested by the Office Action.

1) Chang and Hahm Fail to Disclose or Suggest an Output Pin Coupled to an Output of an Address Control Portion

As noted above, the Office Action asserts that the SMI signal of Chang is equivalent or analogous to the output pin of claim 16. *See Id.*, p. 4. As provided by claim 16, the output pin is coupled to the output of the address control portion that is to indicate a value of an address bit when in the first mode of operation. As further provided by claim 16, the output pin is also coupled to the output of the first data lane enable control portion that is to indicate a first data lane enable value when in the second mode of operation. In contrast, and as noted above, the SMI signal of Chang is an enable signal or a system management interrupt (SMI) signal that is provided by the chipset 220 (Chang, FIG. 2) to the CPU 200 (Chang, FIG. 2) in order to direct the CPU 200 to enter the system management mode (SMM) and to actuate a SMI handler routine. *See Chang*, para. 0031. As also noted above, Chang does not disclose or even suggest that the SMI signal is used to indicate the value of an address bit. Hahm provides no disclosure or suggestion that software interrupt signals provided to a CPU, such as the SMI signal of Chang, are used to provide an address bit of a memory address designating a memory storage location of a memory. Accordingly, the proposed combination of Chang and Hahm fails to disclose or suggest the features of an output pin coupled to the output of an address control portion that is to

indicate the value of an address bit in a first mode of operation and coupled to the output of a first data lane enable control portion that is to indicate a first data lane enable value when in a second mode of operation as provided by claim 16.

2) The Proposed Modification of Chang in view of Hahm Does Not Result in an Output Pin Coupled to a Memory

As provided by claim 16, in addition to being coupled to the outputs of the address control portion and the first data lane enable control portion, respectively, the output pin further is coupled to a memory. Chang discloses that the SMI signal (which the Office Action asserts is analogous to the output pin of claim 16) is connected between the chipset 220 and the CPU 200 (Chang, FIG. 3). Chang provides no disclosure or suggestion that the SMI output of the chipset 220 can be connected to the memory 240. In view of this deficiency in the disclosure of Chang, the Office Action asserts that the system of Chang can be modified in view of the teachings of Hahm to arrive at a system whereby the SMI output of the chipset 220 is coupled to the memory 240. *See Office Action*, p. 4. As discussed above, the SMI signal of Chang is a software interrupt or enable signal that is used to direct the CPU 200 of Chang to enter the SMM mode and to initiate a SMI interrupt handler routine. Hahm merely provides a memory interface that can be integrated into a field programmable gate array (FPGA) and provides no disclosure or suggestion that a software interrupt signal that is provided to a CPU, such as the SMI signal of Chang, also may be provided to a memory. In fact, Hahm does not address interrupt signals in any manner. Accordingly, Chang, as modified by Hahm, still would not disclose or suggest an output pin coupled to an output to indicate a value of an address bit (i.e., the output of the address control portion) and an output to indicate a first data lane enable value (i.e., the output of the first data lane enable control portion) as provided by claim 16. Moreover, not only is the provision of a software interrupt signal not disclosed or suggested by Hahm, one of ordinary skill in the art would appreciate that there is no reason to provide a software interrupt signal to a memory as a conventional memory (which the memories of Chang and Hahm appear to be) does not implement any sort of software processing capability and therefore would have no use for the software interrupt signal.

The Office Action asserts that Hahm renders obvious to one of ordinary skill in the art the integration of "control structure (comprising real mode 100, software interrupt 160, and SMM

180)" into "a single component performing all appropriate functions," such that by "integrating the components in the system of Chang, the outputs of such a system would be directly coupled to the memory 140." *Office Action*, p. 4. The Applicants respectfully submit that the mere integration of the components of the system of Chang into a single device would not affect the interconnection of the components and therefore would not result in the SMIOUT# pin (which provides the SMI signal) being coupled to the memory 240. Instead, if combined into a single device as proposed, the connections between the components of Chang would remain the same absent some motivation provided by Hahm to alter these connections. Hahm fails to provide such motivation. Accordingly, it is respectfully submitted that the proposed combination of Chang and Hahm fails to disclose or suggest the features of an output pin coupled to a memory in addition to the outputs of an address control portion and a first data lane enable portion as recited by claim 16.

3) There is No Motivation to Combine Chang and Hahm

Not only does the proposed combination of Chang and Hahm fail to disclose or suggest features of claim 16, there is no motivation to combine the teachings of Chang and Hahm as discussed in detail above with respect to the rejection of claims 1-5 and 8-10.

4) The Proposed Combination of Chang and Hahm Fails to Disclose or Suggest Each and Every Feature of Claims 16 and 18

As discussed above, there is no motivation to combine the teachings of Chang and Hahm. Even if combined, the proposed combination of Chang and Hahm fails to disclose or suggest at least the features of an output pin coupled an output of an address control portion to indicate a value of an address bit when in a first mode and an output of a first data lane enable control portion to indicate a first data lane enable when in a second mode as recited by claim 16. Moreover, the proposed combination of Chang and Hahm fails to disclose or suggest the features of the output pin being coupled to a memory as recited by claim 16. The Office Action does not assert that the IEEE Dictionary discloses or suggests these features. Accordingly, it is respectfully submitted that the Office Action fails to establish that the proposed combinations of Chang, Hahm and the IEEE Dictionary disclose or suggest each and every feature of claim 16, as well as each and every feature of claims 17 and 18 at least by virtue of their dependency from claim 16. Moreover, these claims recite additional features neither disclosed nor suggested by

Chang, Hahm or the IEEE Dictionary. Consequently, it is respectfully submitted that the obviousness rejections of claims 16-18 are improper at this time and the withdrawal of these rejections therefore is respectfully requested.

Obviousness Rejections of Claims 19 and 20

At page 2 of the Office Action, claim 19 was rejected under 35 U.S.C. Section 103(a) as being unpatentable over Chang in view of Hahm. At page 5 of the Office Action, claim 20 was rejected under 35 U.S.C. Section 103(a) as being unpatentable over Chang in view of Hahm and further in view of the Microsoft Computing Dictionary. These rejections are respectfully traversed.

Claim 19, from which claim 20 depends, recites the features of a memory storing operational instructions that cause a processing module to utilize a first output coupled to the memory to provide a first data lane enable to facilitate accessing of a portion of a first memory storage location of the memory associated with a first memory address when in a first mode of operation, and utilize the first output to provide an address bit of a second memory address to facilitate designation of a second memory storage location of the memory when in a second mode of operation. The Office Action rejects claim 19 under the rational describe above with respect to claim 1. Contrary to the assertions of the Office Action, the Applicants respectfully submit that the proposed combination of Chang and Hahm fails to disclose or suggest each and every feature recited by claims 19 and 20, and further submit that there is no motivation to modify the teachings of Chang in view of Hahm as proposed by the Office Action.

1) Chang and Hahm Fail to Disclose or Suggest an Output that Provides a Data Lane Enable in a First Mode and an Address Bit in a Second Mode

As noted above, the Office Action asserts that the SMI signal of Chang is equivalent or analogous to the first output of claim 1. *See Office Action*, p. 2. As further noted above, Chang teaches the use of the SMI signal to trigger the initiation of the SMM and SMI hander routine at the CPU 200 and Chang does not disclose or even suggest that the SMI signal is used to provide an address bit. Hahm provides no disclosure or suggestion that software interrupt signals provided to a CPU, such as the SMI signal of Chang, are used to provide an address bit of a memory address designating a memory storage location of a memory. Accordingly, the

proposed combination of Chang and Hahm fails to disclose or suggest the features of utilizing a first output to *provide a first data lane enable* for facilitating access of a portion of a first memory location when in a first mode and utilizing the first output to *provide an address bit* of a second memory address when in a second mode as recited by claim 19.

2) The Proposed Modification of Chang in view of Hahm Does Not Result in a First Output Coupled to a Memory

As provided by claim 19, the first output is utilized to provide a first data lane enable in a first mode and to provide an address bit in a second mode is coupled to a memory. As discussed above, the SMI signal of Chang is a software interrupt or enable signal that is used to direct the CPU 200 of Chang to enter the SMM mode and to initiate a SMI interrupt handler routine. As also disclosed above, Hahm provides no disclosure or suggestion that a software interrupt signal that is provided to a CPU, such as the SMI signal of Chang, also may be provided to a memory. As additionally discussed above, not only is the provision of a software interrupt signal not disclosed or suggested by Hahm, one of ordinary skill in the art would appreciate that there is no reason to provide a software interrupt signal to a memory as a conventional memory (which the memories of Chang and Hahm appear to be) does not implement any sort of software processing capability and therefore would have no use for the software interrupt signal.

The Applicants respectfully submit that the mere integration of the components of the system of Chang into a single device as proposed would result in the connections between the components of Chang remaining the same absent some motivation, which Hahm fails to provide. Accordingly, it is respectfully submitted that the proposed combination of Chang and Hahm fails to disclose or suggest the features of a first output coupled to a memory as recited by claim 1.

3) There is No Motivation to Combine Chang and Hahm

Not only does the proposed combination of Chang and Hahm fail to disclose or suggest features of claim 19, as discussed above, there is no motivation to combine the teachings of Chang and Hahm.

4) The Proposed Combination of Chang and Hahm Fails to Disclose or Suggest Each and Every Feature of Claims 19 and 20

As discussed above, there is no motivation to combine the teachings of Chang and Hahm. Even if combined, the proposed combination of Chang and Hahm fails to disclose or suggest at least the features of a memory storing operation instructions that cause a processing module to utilize a first output to provide a first data lane enable when in a first mode and utilize the first output to provide an address bit of a memory address when in a second mode as provided by claim 19. Moreover, the proposed combination of Chang and Hahm fails to disclose or suggest the features of the first output being coupled to a memory as recited by claim 19. The Office Action does not assert that the Microsoft Dictionary discloses or suggests these features. Accordingly, it is respectfully submitted that the Office Action fails to establish that the proposed combination of Chang and Hahm discloses or suggests each and every feature of claim 19, as well as each and every feature of claim 20 at least by virtue of its dependency from claim 19. Moreover, claim 20 recites additional features not disclosed or suggested by the cited references. Consequently, it is respectfully submitted that the obviousness rejections of claims 19 and 20 are improper at this time and the withdrawal of these rejections therefore is respectfully requested.

Obviousness Rejection of Claim 21

At page 2 of the Office Action, claim 21 was rejected under 35 U.S.C. Section 103(a) as being unpatentable over Chang in view of Hahm. This rejection is respectfully traversed.

Claim 21 recites the features of, when in a microcomputer is in a first mode of operation, utilizing a first output coupled to a memory to provide a first data lane enable for facilitating access of a portion of a first memory storage location of the memory associated with a first memory address and, when the microcomputer is in a second mode of operation, utilizing the first output to provide an address bit of a second memory address for facilitating designation of a second memory storage location of the memory. The Office Action rejects claim 21 under the rational describe above with respect to claim 1. Contrary to the assertions of the Office Action, the Applicants respectfully submit that the proposed combination of Chang and Hahm fails to disclose or suggest each and every feature recited by claim 21, and further submit that there is no motivation to modify the teachings of Chang in view of Hahm as suggested by the Office Action.

1) Chang and Hahm Fail to Disclose or Suggest an Output that Provides a Data Lane Enable in a First Mode and an Address Bit in a Second Mode

As noted above, the Office Action asserts that the SMI signal of Chang is equivalent or analogous to the first output of claim 1. *See Office Action*, p. 2. As further noted above, Chang teaches the use of the SMI signal to trigger the initiation of the SMM and SMI hander routine at the CPU 200 and Chang does not disclose or even suggest that the SMI signal is used to provide an address bit. Hahm provides no disclosure or suggestion that software interrupt signals provided to a CPU, such as the SMI signal of Chang, are used to provide an address bit of a memory address designating a memory storage location of a memory. Accordingly, the proposed combination of Chang and Hahm fails to disclose or suggest the features of utilizing a first output to *provide a first data lane enable* for facilitating access of a portion of a first memory location when in a first mode and utilizing the first output to *provide an address bit* of a second memory address when in a second mode as recited by claim 21.

2) The Proposed Modification of Chang in view of Hahm Does Not Result in a First Output Coupled to a Memory

As provided by claim 21, the first output is coupled to memory and utilized to provide a first data lane enable in a first mode and to provide an address bit in a second mode. As discussed above, the SMI signal of Chang is a software interrupt or enable signal that is used to direct the CPU 200 of Chang to enter the SMM mode and to initiate a SMI interrupt handler routine. As also disclosed above, Hahm provides no disclosure or suggestion that a software interrupt signal that is provided to a CPU, such as the SMI signal of Chang, also may be provided to a memory. As additionally discussed above, not only is the provision of a software interrupt signal not disclosed or suggested by Hahm, one of ordinary skill in the art would appreciate that there is no reason to provide a software interrupt signal to a memory as a conventional memory (which the memories of Chang and Hahm appear to be) does not implement any sort of software processing capability and therefore would have no use for the software interrupt signal.

The Applicants respectfully submit that the mere integration of the components of the system of Chang into a single device as proposed would result in the connections between the components of Chang remaining the same absent some motivation, which Hahm fails to provide.

Accordingly, it is respectfully submitted that the proposed combination of Chang and Hahm fails to disclose or suggest the features of a first output coupled to a memory as recited by claim 1.

3) There is No Motivation to Combine Chang and Hahm

Not only does the proposed combination of Chang and Hahm fail to disclose or suggest features of claim 21, as discussed above, there is no motivation to combine the teachings of Chang and Hahm.

4) The Proposed Combination of Chang and Hahm Fails to Disclose or Suggest Each and Every Feature of Claim 21

As discussed above, there is no motivation to combine the teachings of Chang and Hahm. Even if combined, the proposed combination of Chang and Hahm fails to disclose or suggest at least the features of utilizing a first output of a microcomputer to provide a first data lane enable to a memory when the microcomputer is in a first mode and utilizing the first output to provide an address bit of a second memory address to the memory when the microcomputer is in a second mode as provided by claim 21. Moreover, the proposed combination of Chang and Hahm fails to disclose or suggest the features of the first output being coupled to a memory. Accordingly, it is respectfully submitted that the Office Action fails to establish that the proposed combination of Chang and Hahm discloses or suggests each and every feature of claim 21. Consequently, it is respectfully submitted that the obviousness rejection of claim 21 is improper at this time and the withdrawal of this rejection therefore is respectfully requested.

Obviousness Rejection of Claims 11-15

At page 5 of the Office Action, claims 11-15 were rejected under 35 U.S.C. Section 103(a) as being unpatentable over Chang in view of Hahm and further in view of the Microsoft Computer Dictionary. This rejection is respectfully traversed.

1) There is No Motivation to Combine Chang and Hahm

The Office Action rejects claims 11-15 under a similar rationale as the rationale describe above with respect to claims 1, 16, 19 and 21. Contrary to the assertions of the Office Action, as discussed in detail above with respect to claim 1, the Applicants respectfully submit that there is

no motivation to modify the teachings of Chang in view of Hahm as suggested by the Office Action.

2) The Proposed Combination of Chang, Hahm and the Microsoft Computer Dictionary Fails to Disclose or Suggest Each and Every Feature of Claims 11-15

It is respectfully submitted that the Office Action fails to establish that one of ordinary skill in the art would be motivated to combine the teachings of Chang, Hahm and the Microsoft Computer Dictionary to arrive at each and every feature recited by claims 11 ad 15, as well as each and every feature recited by claims 12-14 at least by virtue of their dependency from claim 11. Moreover, claims 12-14 recite additional features not disclosed or suggested by the cited references. Consequently, it is respectfully submitted that the obviousness rejection of claims 11-15 is improper at this time and the withdrawal of this rejection therefore is respectfully requested.

Conclusion

In view of the foregoing, it is respectfully submitted that the present application is in condition for allowance, and an early indication of the same is courteously solicited. The Examiner is respectfully requested to contact the undersigned by telephone at the below listed telephone number in order to expedite resolution of any issues and to expedite passage of the present application to issue, if any comments, questions, or suggestions arise in connection with the present application. The Commissioner is hereby authorized to charge any fees that may be required, or credit any overpayment, to Deposit Account Number 50-2469.

Respectfully submitted,

5 July 2005
Date

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